# DESIGN OF LOGIC GATES USING TOP GATED CARBON NANOTUBE FIELD EFFECT TRANSISTOR

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## ABSTRACT

CNTFET-based devices offer high mobility for near-ballistic transport, high carrier velocity for fast switching, as well as better electrostatic control due to the quasi one-dimensional structure of CNTs. This paper describes the work on modeling, performance benchmarking for nanoscale devices and circuits using carbon Nanotube field effect transistors (CNTFETs), with the aim of guiding nanoscale device and circuit design. In this paper we have successfully developed a compact model for MOSFET like Carbon Nano Tube Field Effect Transistor (CNTFET). The modeled CNTFET has been used to design logic gates which shows superior performance over MOSFET based logic gates and coaxially gated CNTFET logic gates. Hspice simulations have been performed on the designed logic gates and their output behaviors have been extensively studied. Finally a comparison in terms of power consumption and size of the proposed CNTFET vis-à-vis coaxially gated CNTFET and conventional MOSFET has been studied.

**Key words** Carbon Nanotube (CNT), CNT Field Effect Transistor (CNTFET), Chiral Vector, Coaxially gated, Compact modeling, logic gates, MOSFET.

## I. INTRODUCTION

For many years MOSFET has been used as a basic element of circuit designing[1]. As the miniaturization of silicon based circuits reaches its physical limitations, molecular devices are becoming hopeful alternatives to the existing silicon technology [2][3]. Carbon Nano Tube (CNT) technology is at the front of these technologies due to the unique mechanical and electronic properties. Semi- conducting carbon nanotube can be used as the channel in Carbon Nanotube Field Effect Transistor (CNTFET).

CNTFETs are novel devices that are expected to sustain the transistor scalability while increasing its performance. One of the major differences between CNTFETs and MOSFETs is that the channel of the former devices is formed by CNTs instead of silicon, which enables a higher drive current density, due to the larger current carrier mobility in CNTs compared to bulk silicon[4]-[6]. The main drawbacks of the MOSFET is that the sensitivity of a MOSFET's gate to static and high-voltage spikes makes it vulnerable to damage resulting from parasitic oscillation. This undesired self-oscillation could result in excessive gate-to-source voltage that permanently damages the MOSFET's gate insulation. Another MOSFET limitation is gate capacitance. This parameter limits the frequency at which a MOSFET can operate effectively. CNTFET overcomes these limitations to produce better performance than MOSFET.

In this paper, section II Introduces the Carbon nanotubes, their background, the underlying physics and electronic structure of the CNT. Section III and Section IV delves into the structure and modeling aspects of MOSFET like CNTFET. Simulation results of various benchmark circuits such as AND, OR, NOT, NAND and XOR gates [7] have been discussed in section V. Finally in section VI, the research paper has been concluded with the work undertaken in this research work and the scope for improvement of the circuit level transistor models.

## II. CARBON NANOTUBE ELECTRONICS

Carbon nanotubes were discovered by S. Ijiima[8] in 1991 while performing some experiments on molecular structure composed of carbonium. CNTs are hollow cylinders composed of one or more concentric layers of carbon atoms in a honey comb lattice arrangement[9]-[12]. It can be classified into SWCNT (Single Walled Carbon Nano Tube) and MWCNT (Multi Walled Carbon Nano Tube) shown in Figure 1.

Based on the chiral vector, Circular vector that is perpendicular to the axis of the tube, CNTs are classified into Arm Chair, Zigzag & Chiral as shown in Figure 2. CNTs can be either metallic or

semiconducting; this raises the scope for new integrated circuit technologies made from CNT transistors and interconnects. However, in this research we confine our study to CNT Field Effect Transistor.

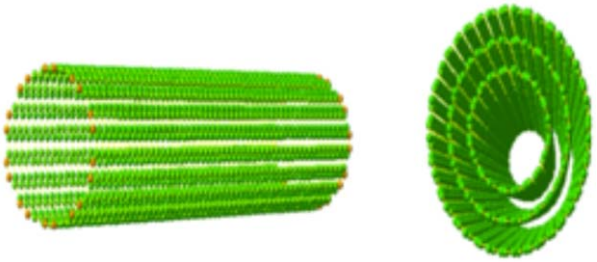

Fig. 1. SWCNT and MWCNT

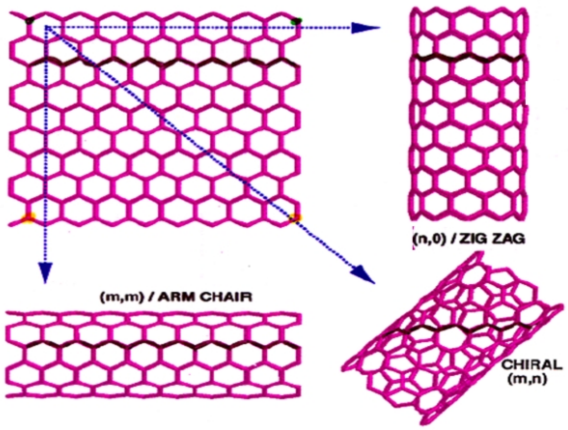


Fig. 2. Classification based on chiral vector

## III. CARBON NANOTUBE FIELD EFFECT TRANSISTOR

It has been shown that semiconducting carbon nanotubes can be used as the conducting channel in Carbon nanotube field effect transistors. To create such devices, nanotubes are grown on top of a thick silicon dioxide. When metal contacts are laid along the length of a nanotube, many transistors are formed along CNT. The length of the nanotube, between two contacts, acts as the channel of a transistor with metal source and drain. Because of the fixed CNT diameter once a nanotube is grown, the width of the nanotube cannot be changed to increase the current drive, instead, a transistor's width and current drive can be increased by adding nanotubes in parallel.

The metal gate is used to modulate the electronic band structure of the source, drain and carbon nanotube through a thin gate oxide. The metal gate and oxide must overlap slightly with the source and drain contacts. This overlap limits the area savings of CNTFETs. The current is regulated by the gate to source and gate to drain interactions. Figure 3 is a theoretical illustration of a carbon nanotube FET structure. The structure resembles that of a MOSFET[13]-[15], but the nanotube is the channel for conduction.

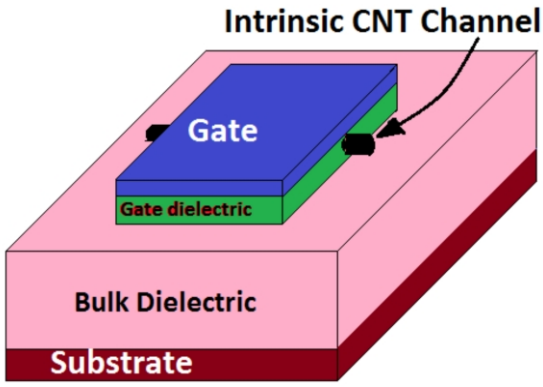


Fig. 3. Structure of MOSFET like CNTFET

## IV. SIMULATION MODEL OF CNTFET

The MOSFET-like CNTFET model used in this study is schematically shown in Figure 4. A brief description of the theoretical analysis is given as follows. We assume near-ballistic transport and contacts in this work, i.e. $eV_{DS} \approx \mu_d - \mu_s$ so $\mu_s$ remains almost constant in the source-channel region and $\mu_d$ remains almost constant in the channel-drain region.

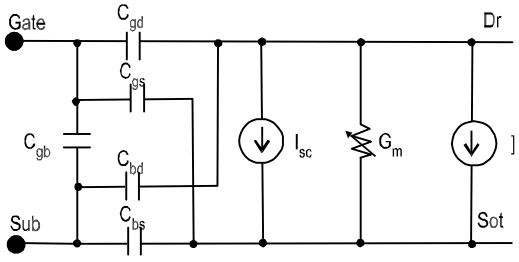


Fig. 4. Equivalent circuit of MOSFET like CNTFET

We consider three current sources in this CNTFET model: 1. the thermionic current contributed by the semiconducting sub-bands ($I_{semi}$) with the classical band theory, 2. the current contributed by the metallic sub-bands ($I_{metal}$), and 3. the leakage current ($I_{btbt}$) caused by the band to band tunneling mechanism through the semiconducting sub-bands.

### *A. Current and Capacitance Expressions*

The thermionic current contributed by the semi conducting sub-bands is given by,

$$I_{semi}(V_{ch,DS}, V_{ch,GS}) = \frac{4e^2}{h}\sum_{\substack{k_m \\ m=1}}^{M} T_m - \left[ V_{ch,GS} + \frac{kT}{e} \ln\left( \frac{1 + e^{(K_{m,0} - \Delta\Phi_g)/KT}}{1 + (E_{m,0} - \Delta\Phi_g + eV_{ch,Ds})/KT} \right) \right] \quad [1]$$

$V_{ch,DS}$ and $V_{ch,GS}$ denotes the Fermi potential differences near source side within the channel, e is the unit electronic charge, $\Delta\Phi_B$ is the channel surface potential change with gate/drain bias, Tm is the transmission probably, k is the Boltzmann constant and T is the temperature in Kelvin and $E_{m,0}$ is the half band gap of the mth sub-band.

For metallic sub-bands of metallic nanotubes, the current $I_{metal}$ includes both the electron current and the hole current,

$$I_{metal} = 2(1 - m0)\, T_{metal} \sum_{\substack{k_t \\ l=1}}^{L} [J_{ele\_0,t} + J_{hole\_0,t}] \quad [2]$$

$$J_{ele\_0.1} = \frac{2e}{h} \frac{\sqrt{3a}\,\pi V_\pi}{L_g} (f_{FD}(E_{0,t} - \Delta\Phi_B) - f_{FD}(E_{0,t} + eV_{ch,DS} - \Delta\Phi_B)) \quad [3]$$

$$J_{hole\_0,t} = \frac{2e}{h} \frac{\sqrt{3a}\pi V_s}{L_g} (f_{FD}(-E_{0,t} - \Delta\Phi_B) - f_{FD}(-E_{0,t} + eV_{ch,DS} - \Delta\Phi_B)) \quad [4]$$

$f_{FD}(E)$ is the Fermi-Dirac distribution function, $f_{FD}(E) = \dfrac{1}{1 + e^{E/KT}}$ and the transmission probability $T_{metal}$ is given by,

$$T_{metal} = \frac{\lambda_{ap}\lambda_{op}}{\lambda_{ap}\lambda_{op} + (\lambda_{ap} + \lambda_{op}) \cdot L_g} \quad [5]$$

$L_g$, the channel length , $\lambda_{op}$ (~ 15 nm[16]), the optical phonon scattering mean free path (MFP) and $\lambda_{ap}$ (~ 500 nm [17]), the acoustic phonon scattering MFP.

In the sub-threshold region, especially with negative gate bias (nFET), the band-to-band tunneling current from drain to source becomes significant. We include a voltage controlled current source $I_{bt}$ in the device model in order to evaluate the device sub-threshold behavior and the static power consumption.

$$I_{btbt} = \frac{4e}{h} KT \sum_{\substack{k_m \\ m=1}}^{\cdot} T_{btbt} \ln\left[ \left( 1 + \frac{e^{(eV_{ch,DS} - E_{m,0} - E_f)/KT}}{1 + (E_{m,0}} - E_f)/KT \right) \frac{\max(eV_{ch,DS} - 2E_{m,n}, 0)}{eV_{ch,DS} - 2E_{m,0}} \right] \quad [6]$$

To model the intrinsic ac response of CNTFET device, we use a controlled transcapacitance array among the four electrodes (G, S, D, B) with the Meyer capacitor model[18], thereby the equations for capacitance calculation are given as follows.

$$C_{bd} = C_{gd} \frac{C_{sub}}{C_{ox}} \quad [7]$$

$$C_{bs} = C_{gs} \frac{C_{sub}}{C_{ox}} \quad [8]$$

$$C_{gd} = \frac{L_g C_{ox}(C_{QS} + \beta(C_c)}{C_{tot} + C_{Qs} + C_{Qd}} \quad [9]$$

$$C_{gs} = \frac{L_g C_{ox}(C_{Qs} + (1 - \beta C_c))}{C_{tot} + C_{Qs} + C_{Qd}} \quad [10]$$

$$C_{bg} = C_{gb} = \frac{L_g C_{sub} C_{ox}}{C_{tot} + C_{Qs} + C_{Qd}} \quad [11]$$

$C_{tot}$, is the total electrostatic coupling capacitance per unit length between channel and other electrodes, $C_{Qs}$ and $C_{Qd}$ as the quantum capacitance due to the carriers from source (+ k branch) and drain (–k branch), respectively.

## V. SIMULATION RESULTS AND DISCUSSIONS

In order to demonstrate the versality of MOSFET like CNTFET, we employed it to design basic logic gates. A logic gate is an electronic circuit/device which makes the logical decisions. To arrive at this decisions, the most common logic gates used are OR, AND, NOT, NAND and NOR gates. The NAND and NOR gates are called universal gates. The exclusive-OR gate is another logic gate which can be constructed using AND, OR and NOT gate.

### *A. NOT GATE*

Figure 5 shows an exemplary logic gate (inverter) comprising of P-type and N-type CNTFETs. They are

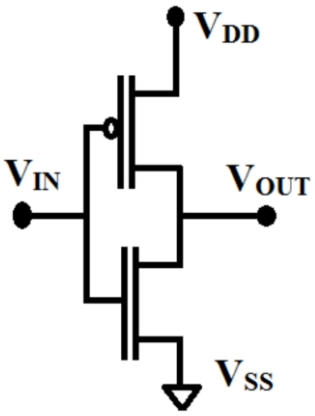


Fig. 5. Structure of NOT gate

coupled together in series between a high supply voltage ($V_{DD}$) and a low supply reference $V_{SS}$, as shown. The first CNTFET which is biased to conduct holes, functions as a driver transistor with its gate providing an inverter input $V_{IN}$. The second transistor which is biased to conduct electrons, functions to facilitate an active load with its gate coupled to a supply VGG for appropriately biasing it, so that the output provides suitable low and high values when $V_{IN}$ is high and low respectively as shown in Figure 6.

### *B. NAND GATE*

Figure 7 shows an exemplary NAND gate comprising of CNTFETs as discussed herein in accordance with some embodiments. It comprises of driver CNTFETs coupled together in parallel between a high supply reference ($V_{DD}$) and a series active load

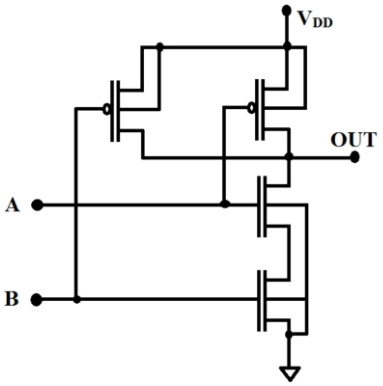


Fig. 7. Structure of NAND gate

transistors, which is coupled to a low supply reference $V_{SS}$, as shown.

The gates of the driver transistors provide first and second NAND gate inputs respectively and a gate output is provided at the drain of third transistor as shown. If either input or any one of the input is Low (e.g., 0V) then the output is High (approaching VDD), if both inputs are high, then the output will be Low as shown in Figure 8.

### *C. NOR GATE*

Figure 9 shows an exemplary NOR gate comprising of CNTFETs as discussed herein in accordance with some embodiments. It comprises of driver CNTFETs coupled together in series between a high supply reference ($V_{DD}$) and a parallel connected active load transistors, which is coupled to a low supply reference $V_{SS}$, as shown.

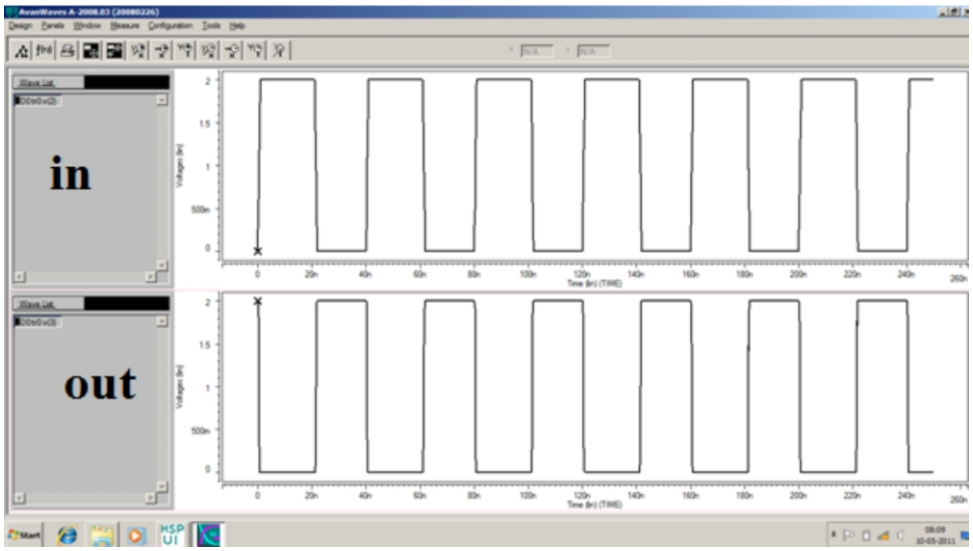


Fig. 6. Behavior of NOT gate

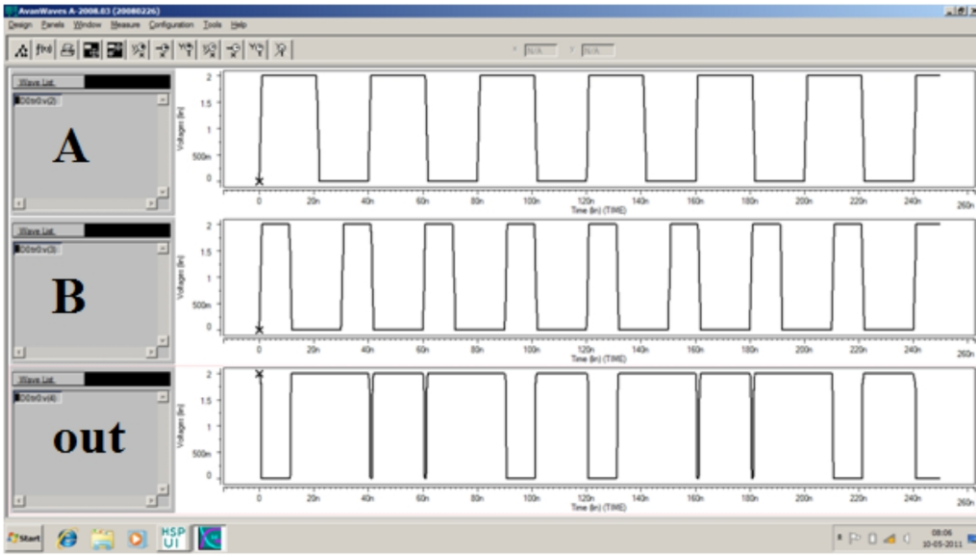


Fig. 8: Behavior of NAND gate

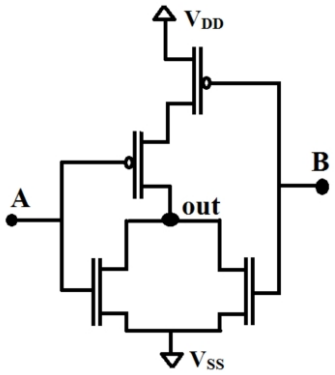


Fig. 9. Structure of NOR gate

The gates of the driver transistors provide first and second NOR gate inputs respectively and a gate output is provided at the drain of parallel combination as shown. If either input is Low (e.g., 0V) then the output is High (approaching $V_{DD}$), conversely, if both inputs are high (approaching $V_{DD}$), then the output will be Low as shown in Figure 10.

### *D. AND GATE*

The AND gate performs logical multiplication, commonly known as AND function. The AND gate shown in Figure 11 has two or more inputs and single output. The HIGH (i.e. even if one input is LOW, Output

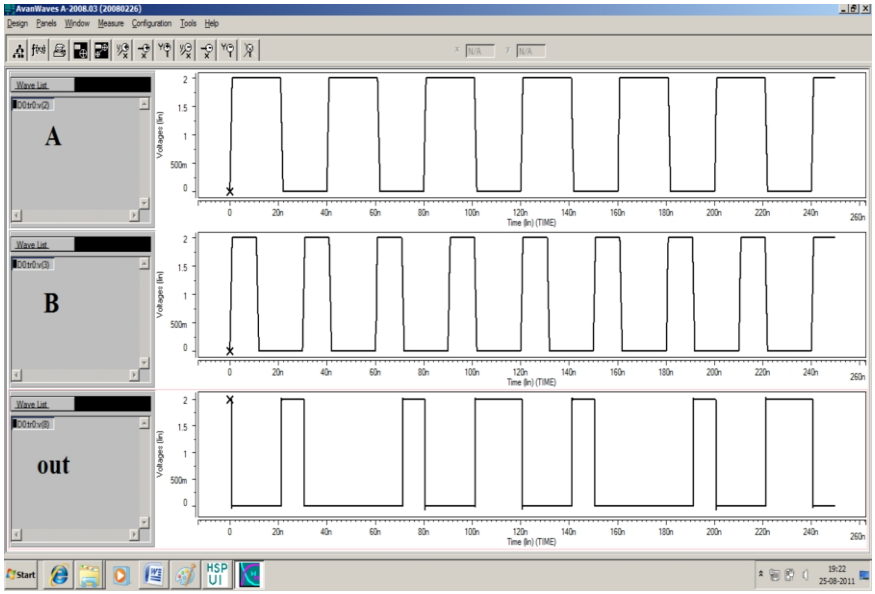


Fig. 10. Behavior of NOR gate

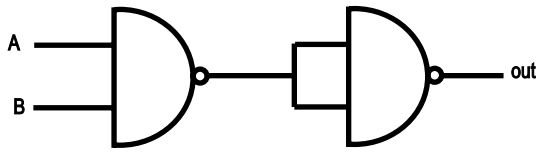


Fig. 11. Structure of AND gate

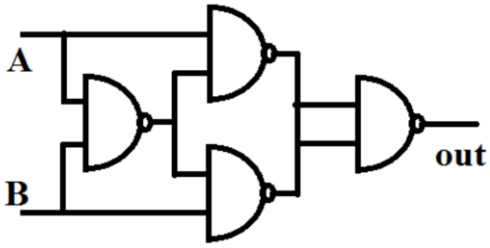


Fig. 13. Structure of XOR gate

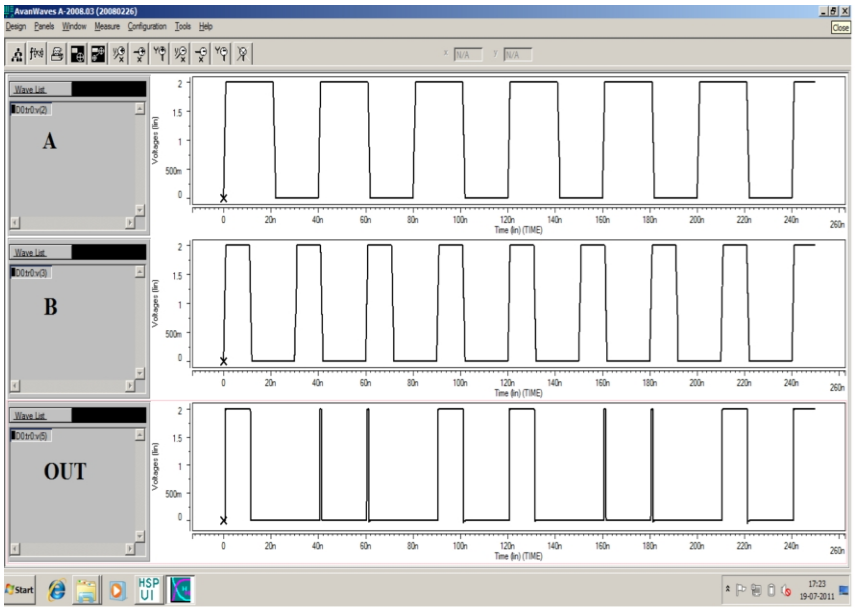


Fig. 12. Behavior of AND gate

will be LOW). If X and Y are two inputs, then output F can be represented mathematically as F = X.Y, Here dot (.) denotes the AND operation. Figure 12 shows the behavior of output of AND gate is HIGH only when all its inputs are AND gate.

### *E. XOR GATE*

An Exclusive-OR (XOR) gate is gate with two or three or more inputs and one output. The output of a two-input XOR gate assumes a HIGH state if one and only one input assumes a HIGH state. This is equivalent to saying that the output is HIGH if either input X or input Y is HIGH exclusively and LOW when both are 1 or 0 simultaneously. If X and Y are two inputs, then output F can be represented mathematically as $F = X \oplus Y$, Here $\oplus$ denotes the XOR operation. $X \oplus Y$ and is equivalent to $X \cdot Y' + X' \cdot Y$.

Figure 13 and Figure 14 shows the structure and behavior of XOR gate.

### *F. OR GATE*

The OR gate performs logical addition, commonly known as OR function. The OR gate shown in Figure 15 has two or more inputs and single output. The output of OR gate is HIGH only when any one of its inputs are HIGH (i.e. even if one input is HIGH, Output will be HIGH). If X and Y are two inputs, then output F can be represented mathematically as F = X + Y. Here plus sign (+) denotes the OR operation. Figure 16 shows the behavior of AND gate.

## VI. CONCLUSION

The compact model has been developed for the MOSFET like Carbon Nanotube Field Effect Transistor. Simulation results of various benchmark circuits such as NOT, NAND and NOR gates has been discussed. A comparison has been made between the coaxially gated CNTFET and MOSFET like CNTFET which shows that, though good dc current can be achieved by SB-controlled CNTFET with the self-aligned

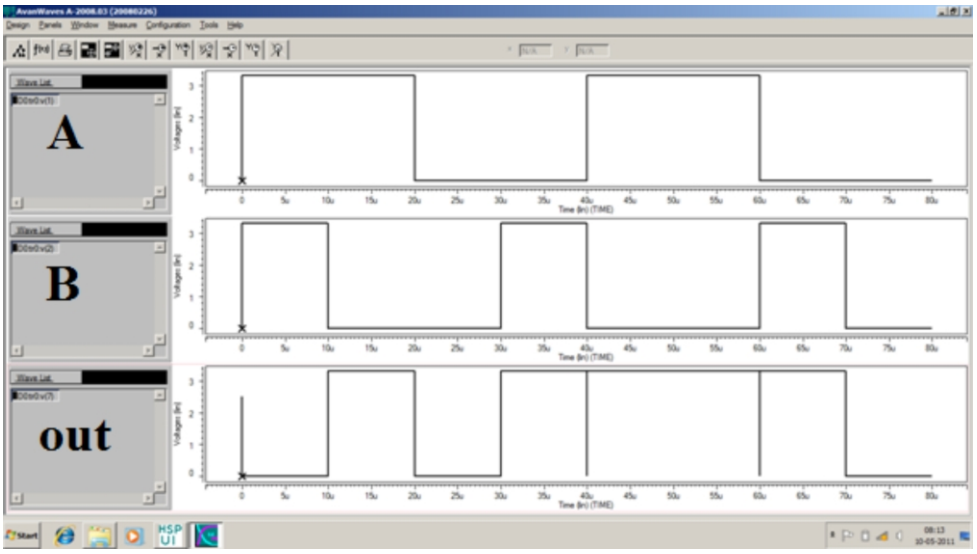


Fig. 14. Behavior of XOR gate

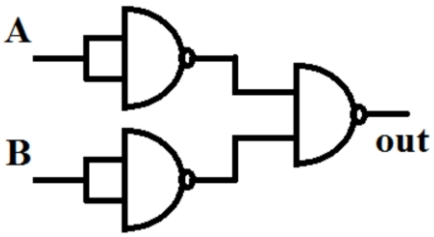


Fig. 15. Structure of OR gate

structure, its ac performance is poor due to the proximity of the gate electrode to the source/drain metal. The ambipolar behavior of SB-controlled CNTFET also makes it undesirable for complementary logic design. The fabrication feasibility and superior device performance of the MOSFET-like CNTFET as compared to the SB-controlled FET leads to reduction in the power dissipation factor and also the device size.

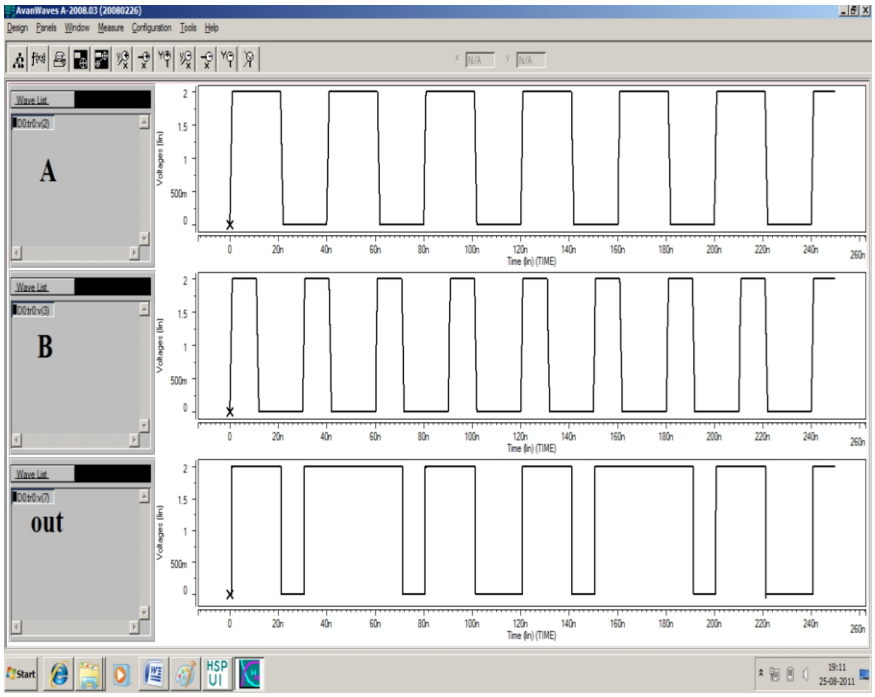


Fig. 16. Behavior of OR gate

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